

Fig. 1

code	country	area	pop	gdp	gdp/cap	pop	area	pop	gdp	gdp/cap
001	Algeria	238147	14000000	1000000000	714	002	Angola	480000	1000000000	2083
003	Argentina	278016	35000000	10000000000	2857	004	Armenia	29743	10000000	339
005	Australia	774122	19000000	10000000000	5263	006	Austria	83858	8000000	9528
007	Azerbaijan	86600	7000000	100000000	1428	008	Bahrain	653	1000000	10000
009	Bangladesh	147570	120000000	1000000000	83	010	Barbados	430	280000	6471
011	Belarus	207600	10000000	1000000000	482	012	Belgium	30528	10000000	32687
013	Belgium	30528	10000000	1000000000	32687	014	Belize	22696	400000	1785
015	Belize	22696	400000	100000000	2462	016	Bhutan	38394	250000	650
017	Bolivia	366127	9000000	1000000000	111	018	Bosnia and Herzegovina	51129	4000000	782
019	Bolivia	366127	9000000	1000000000	111	019	Bosnia and Herzegovina	51129	4000000	782
020	Brazil	851196	170000000	10000000000	588	021	Brazil	851196	170000000	588
021	Brazil	851196	170000000	10000000000	588	022	Bulgaria	110879	8000000	723
022	Bulgaria	110879	8000000	1000000000	723	023	Burkina Faso	274000	12000000	420
023	Burkina Faso	274000	12000000	1000000000	420	024	Burkina Faso	274000	12000000	420
024	Burkina Faso	274000	12000000	1000000000	420	025	Burkina Faso	274000	12000000	420
025	Burkina Faso	274000	12000000	1000000000	420	026	Burkina Faso	274000	12000000	420
026	Burkina Faso	274000	12000000	1000000000	420	027	Burkina Faso	274000	12000000	420
027	Burkina Faso	274000	12000000	1000000000	420	028	Burkina Faso	274000	12000000	420
028	Burkina Faso	274000	12000000	1000000000	420	029	Burkina Faso	274000	12000000	420
029	Burkina Faso	274000	12000000	1000000000	420	030	Burkina Faso	274000	12000000	420
030	Burkina Faso	274000	12000000	1000000000	420	031	Burkina Faso	274000	12000000	420
031	Burkina Faso	274000	12000000	1000000000	420	032	Burkina Faso	274000	12000000	420
032	Burkina Faso	274000	12000000	1000000000	420	033	Burkina Faso	274000	12000000	420
033	Burkina Faso	274000	12000000	1000000000	420	034	Burkina Faso	274000	12000000	420
034	Burkina Faso	274000	12000000	1000000000	420	035	Burkina Faso	274000	12000000	420
035	Burkina Faso	274000	12000000	1000000000	420	036	Burkina Faso	274000	12000000	420
036	Burkina Faso	274000	12000000	1000000000	420	037	Burkina Faso	274000	12000000	420
037	Burkina Faso	274000	12000000	1000000000	420	038	Burkina Faso	274000	12000000	420
038	Burkina Faso	274000	12000000	1000000000	420	039	Burkina Faso	274000	12000000	420
039	Burkina Faso	274000	12000000	1000000000	420	040	Burkina Faso	274000	12000000	420
040	Burkina Faso	274000	12000000	1000000000	420	041	Burkina Faso	274000	12000000	

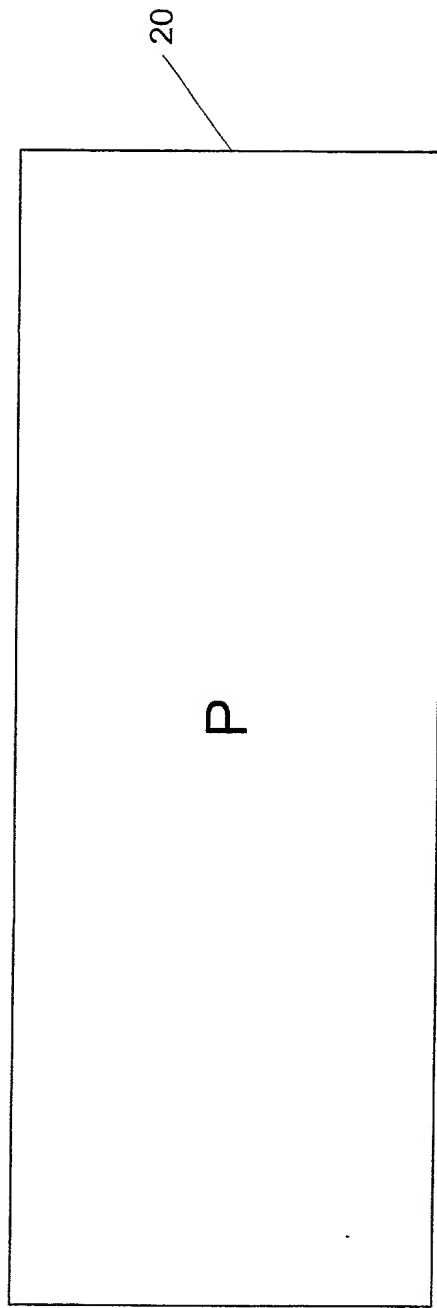


Fig. 2a

FIG. 2b is a schematic diagram of a semiconductor device 20, showing a cross-sectional view of a substrate 22 with an epitaxial layer (EPI) and a p-type region (P). A circular feature 29 is located within the p-type region.

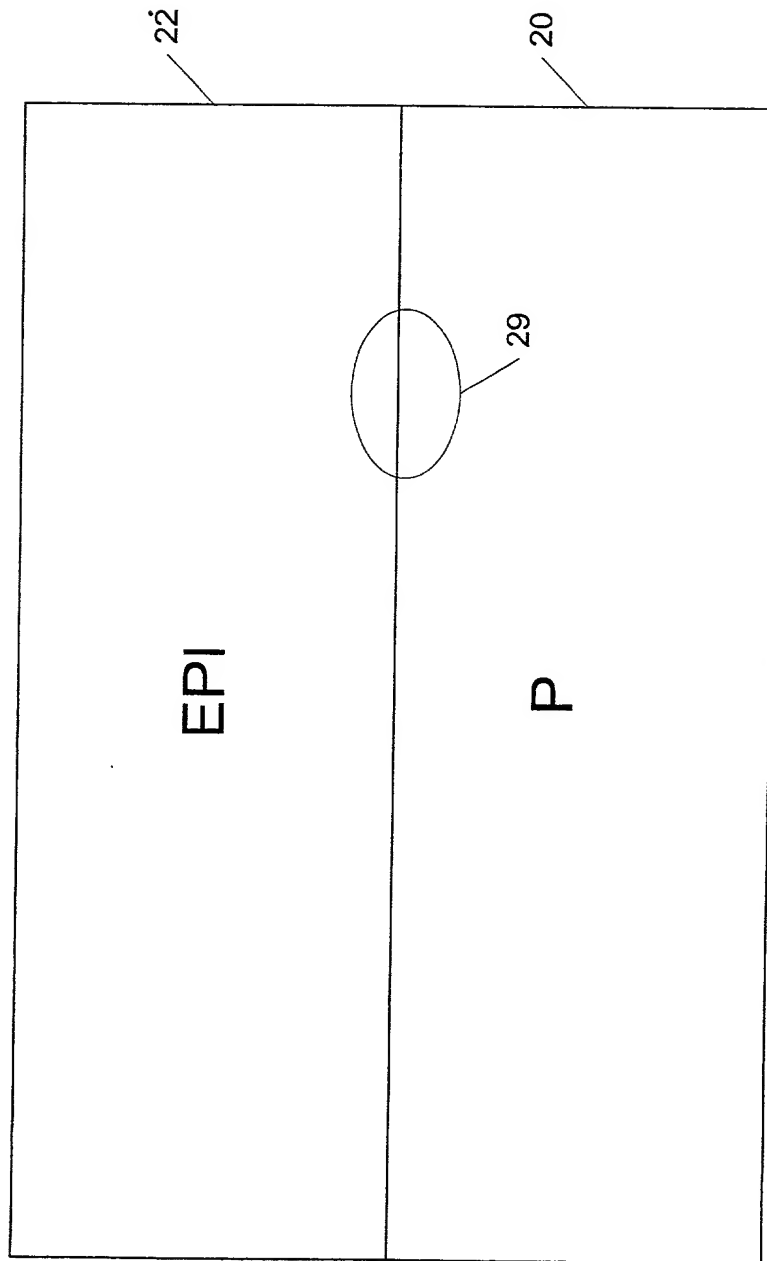


Fig. 2b

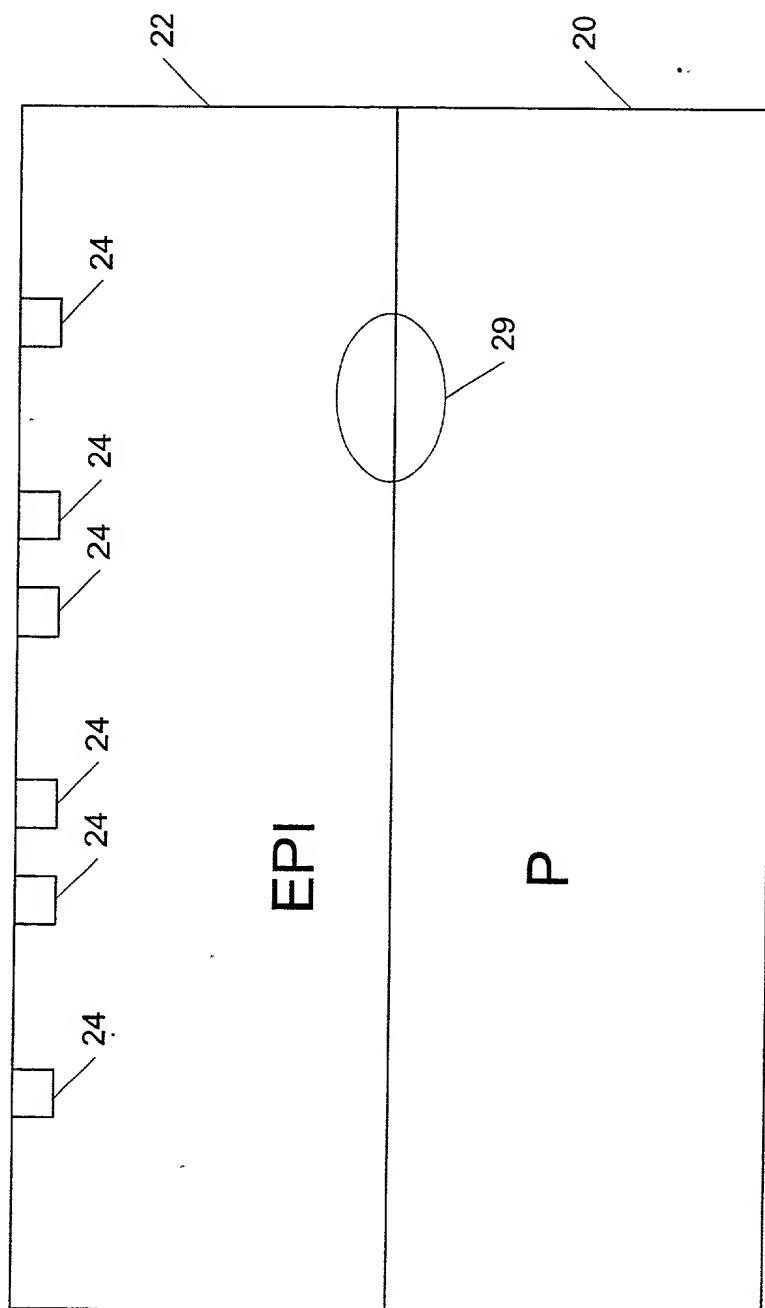


Fig. 2c



FIG. 2e is a cross-sectional view of the device of FIG. 2d, taken along line 2e-2e of FIG. 2d. The device includes a substrate 20, a P-type region 22, and an EPI layer 24. The EPI layer 24 is formed on the P-type region 22. The device also includes a gate stack 26, which is formed on the EPI layer 24. The gate stack 26 includes a gate oxide layer 27 and a gate electrode 28. The gate electrode 28 is formed on the gate oxide layer 27. The device also includes a source/drain region 29, which is formed in the EPI layer 24. The source/drain region 29 is formed by implanting dopants into the EPI layer 24. The source/drain region 29 is located under the gate stack 26. The device also includes a contact 30, which is formed on the source/drain region 29. The contact 30 is formed by depositing a conductive material on the source/drain region 29. The contact 30 is used to connect the source/drain region 29 to an external circuit.

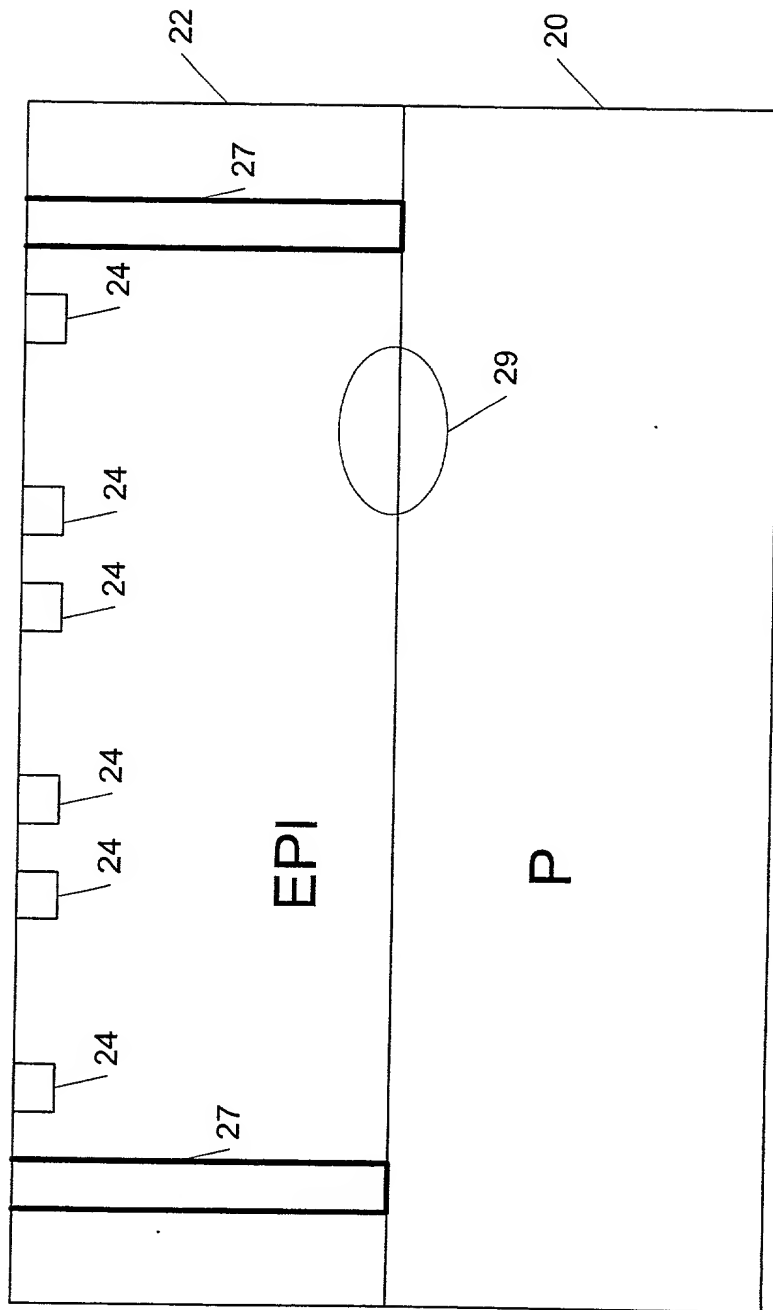


Fig. 2e

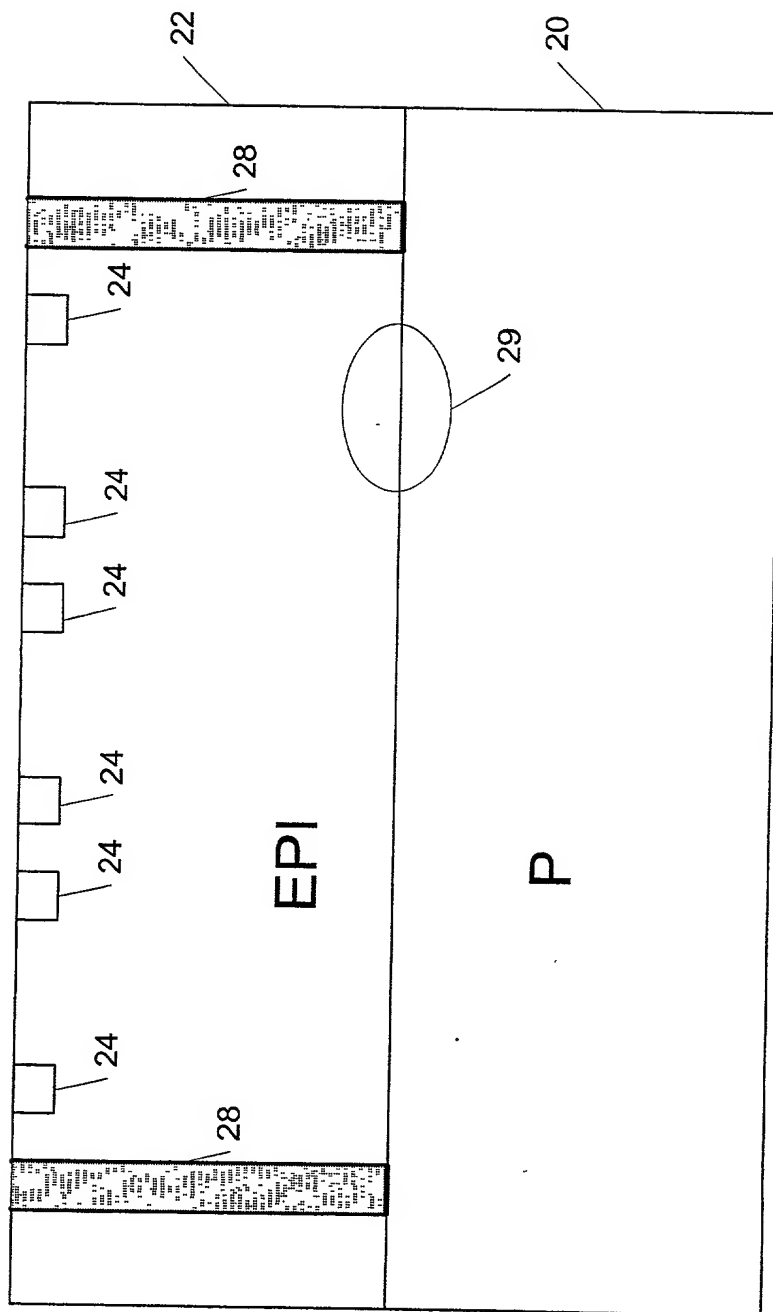


Fig. 2f

Figure 29g shows a cross-sectional view of a semiconductor device. The device includes a substrate 20, a p-type layer 33, and an n-type layer 28. A gate stack 24 is formed on the substrate 20, and a gate electrode 22 is formed on the gate stack 24. A source/drain region 29 is formed in the substrate 20, and a source/drain contact 31 is formed on the source/drain region 29. The device is labeled EPI.

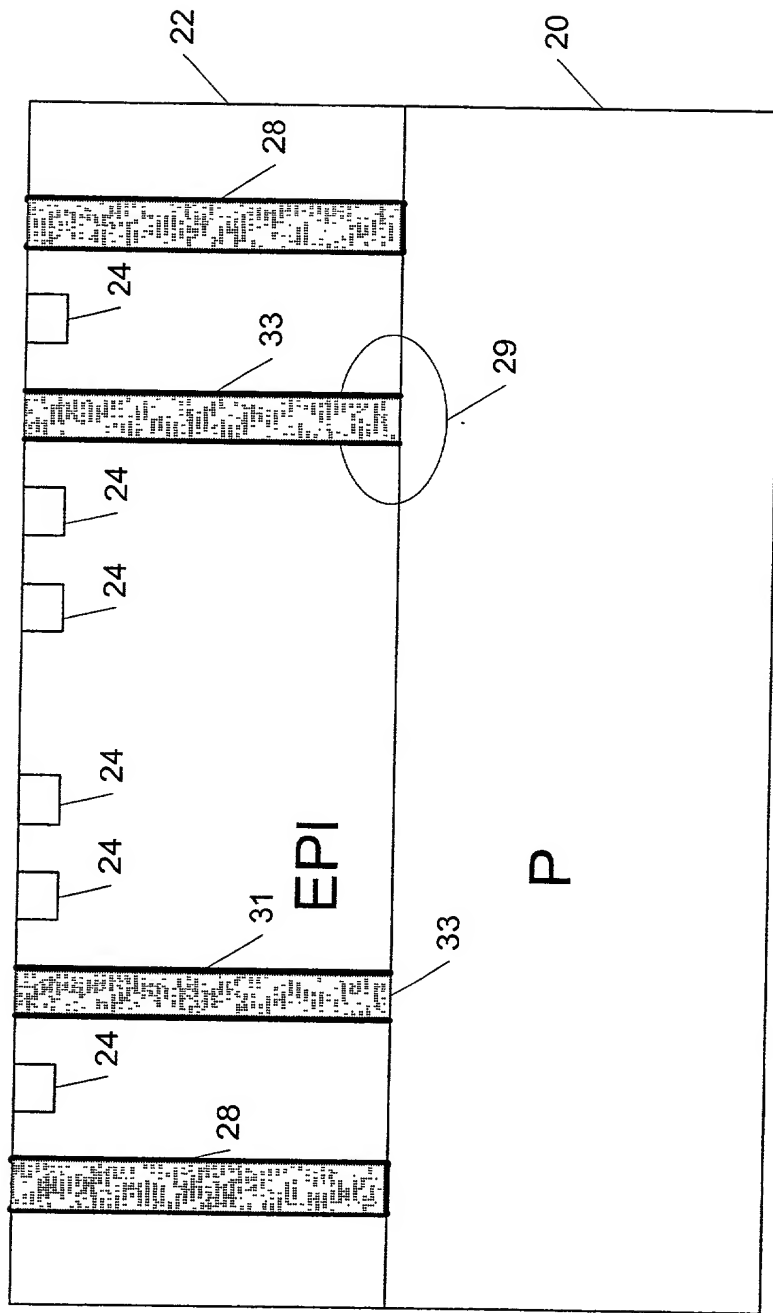


Fig. 29g



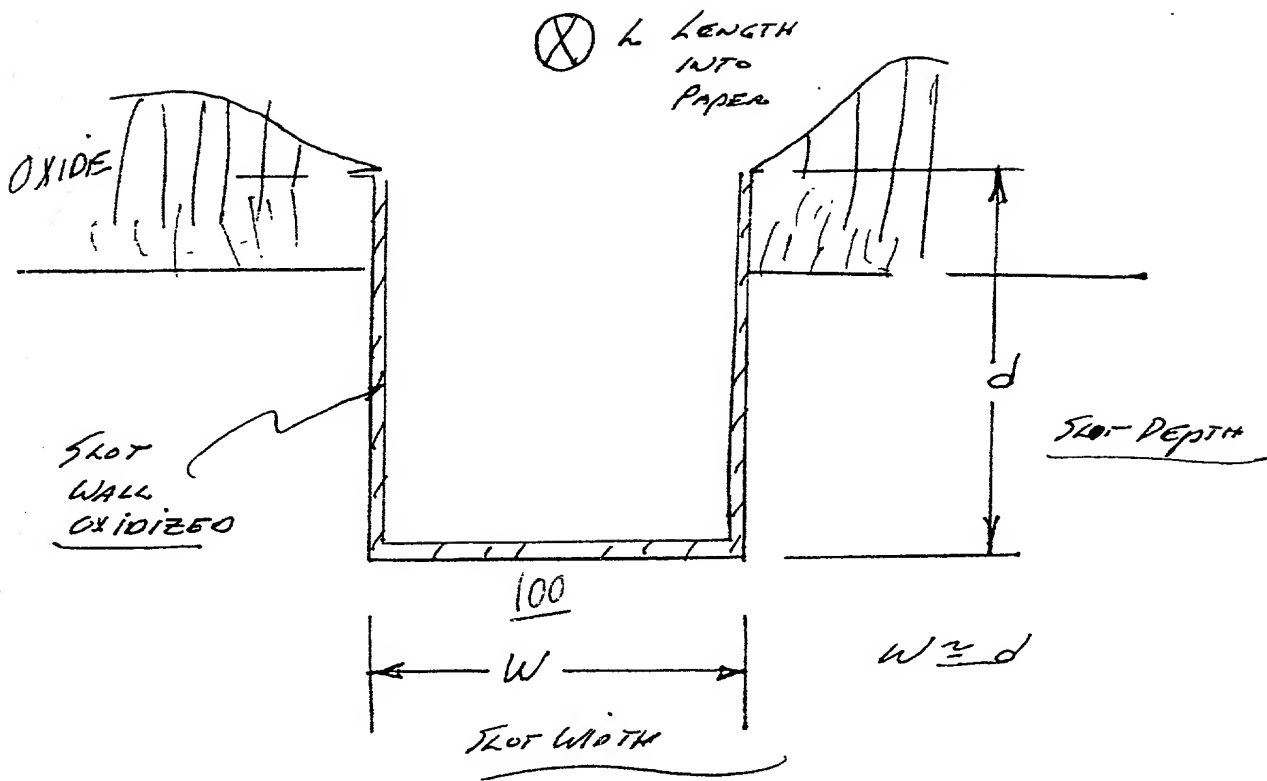


Fig. 3

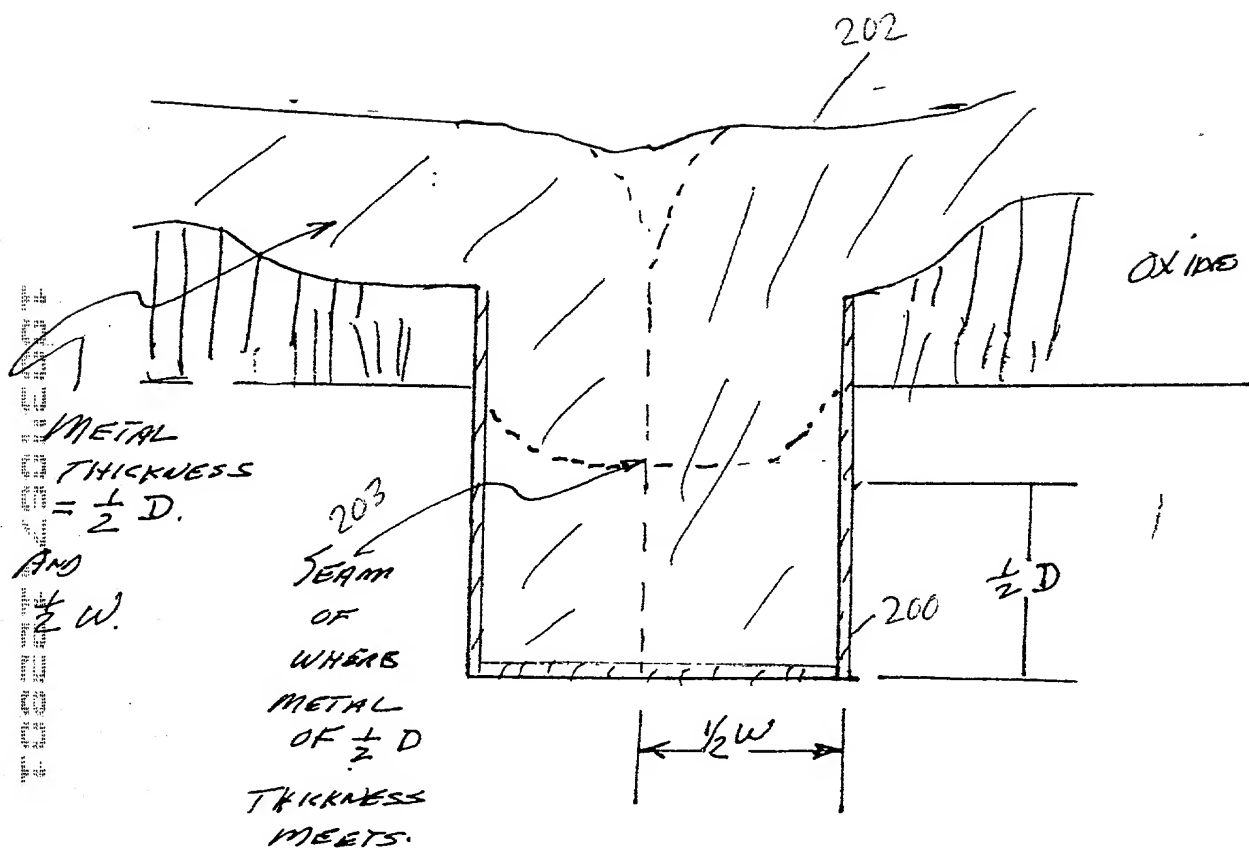
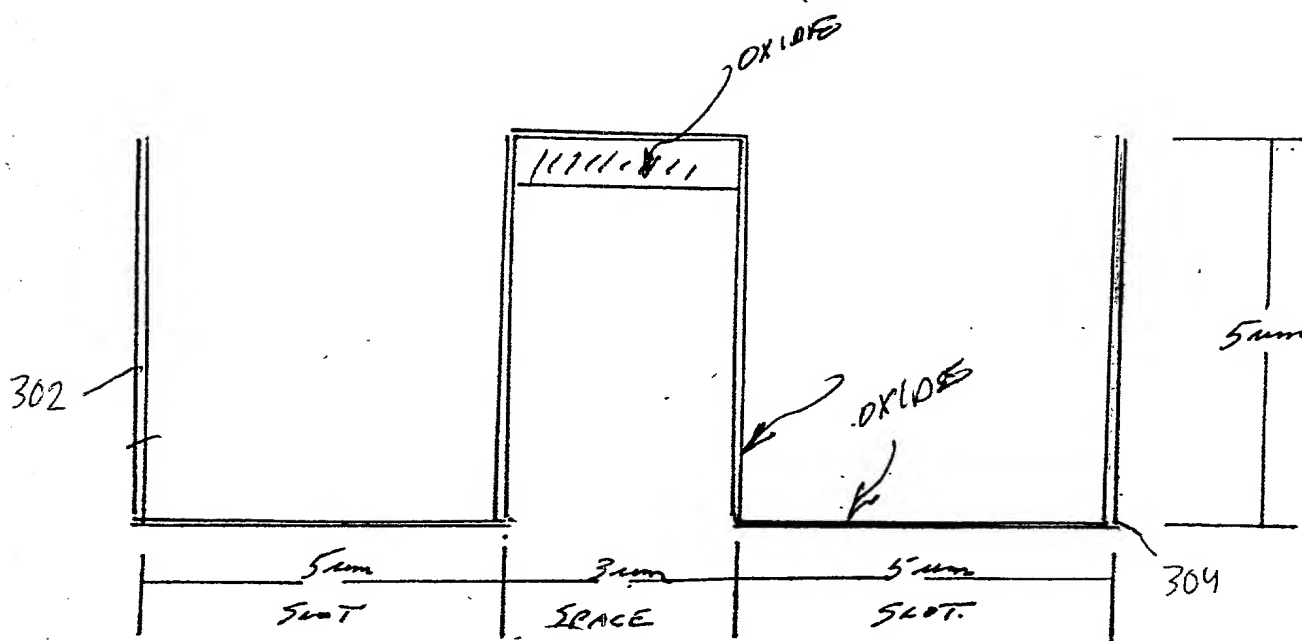
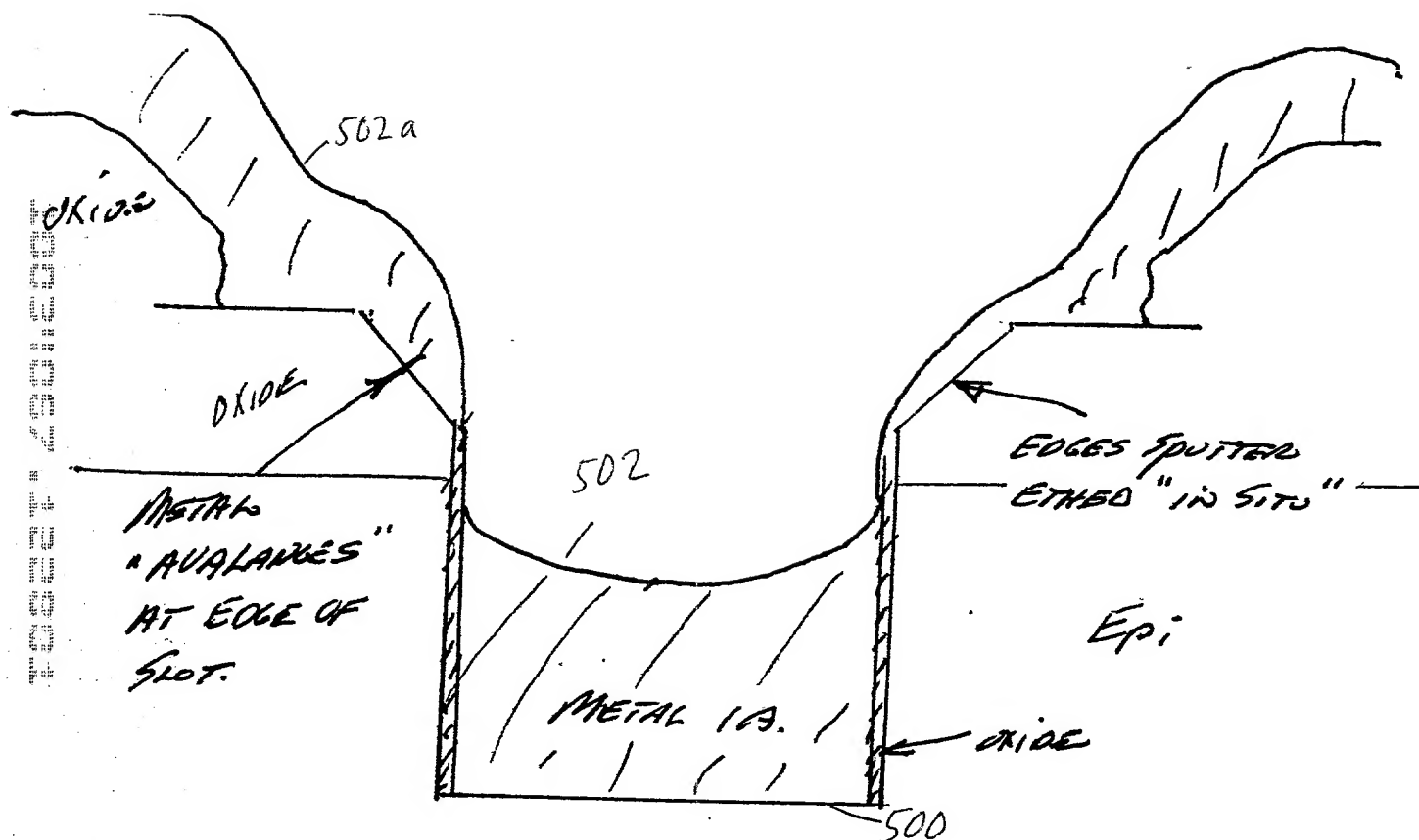


Fig. 4



DOUBLE SLOT FOR  
DOUBLE WIDTH OF METAL.  
3mm SPACE BETWEEN SLOTS

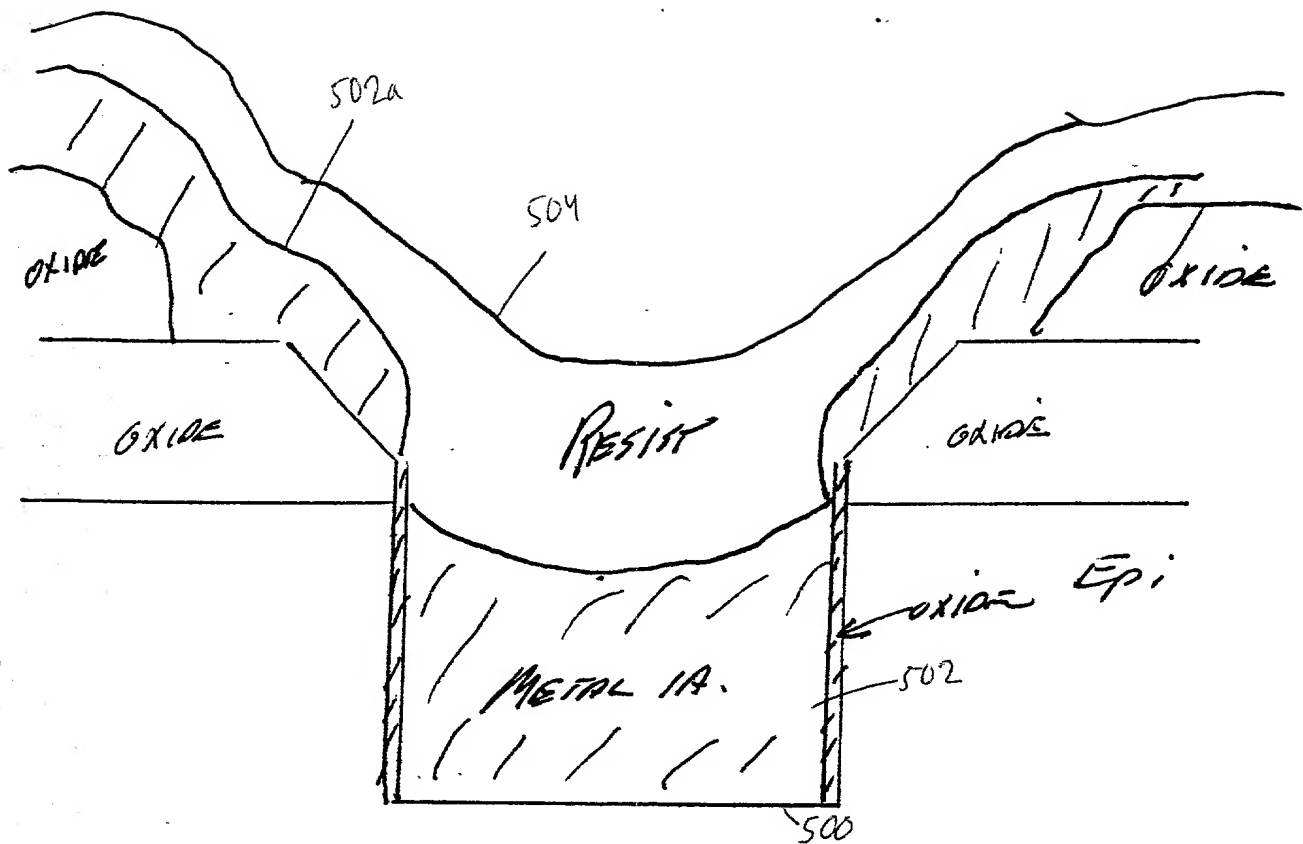
Fig. 4a



Prior TO METAL 1A BEING  
 SPUTTERED, THE EDGES OF THE OXIDES  
 ARE SPUTTERED ETCHED "IN SITU" &  
 1A DEPOSITED

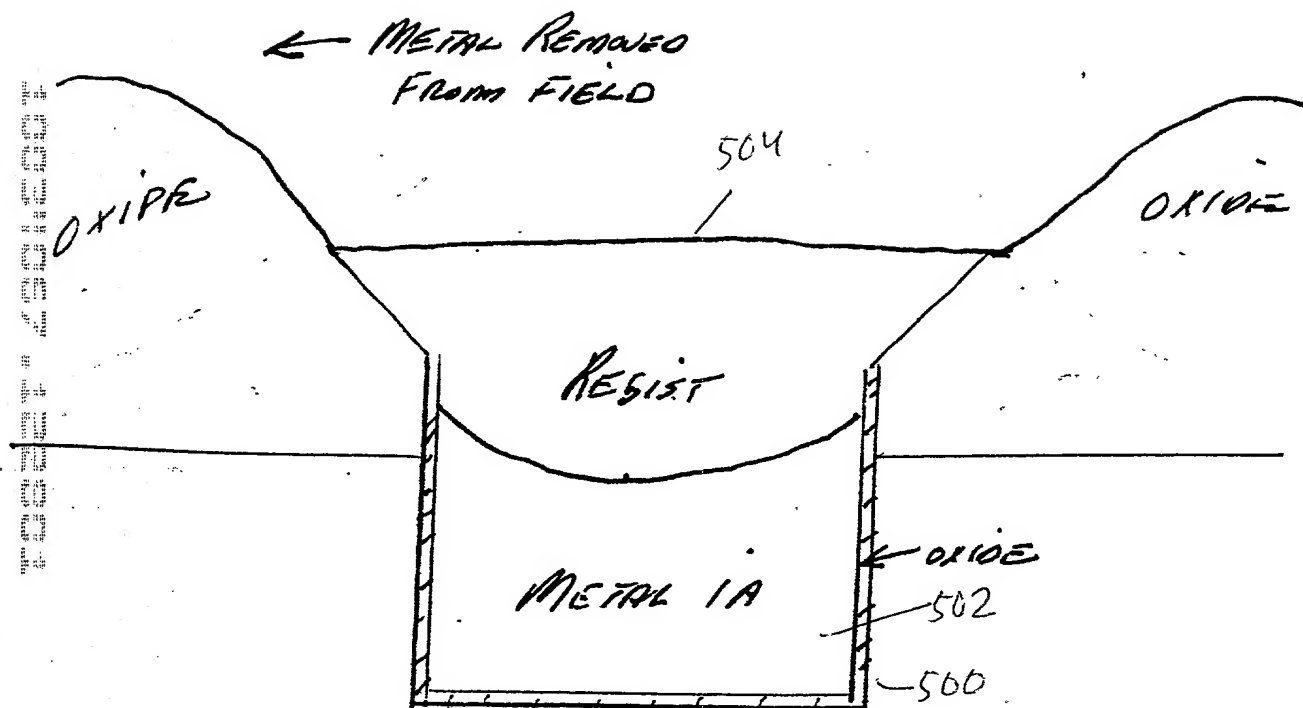
Fig. 5

It is a drawing of a cross-section of a semiconductor device. It shows a substrate with a metal layer (500) and an oxide layer (502). A resist layer (504) is applied over the oxide layer, and it is thicker in the slots (502a). The oxide layer is labeled 'OXIDE' and 'OXIDE Epi'. The metal layer is labeled 'METAL 1A.'. The resist layer is labeled 'RESIST'. The slots are labeled '502a'.



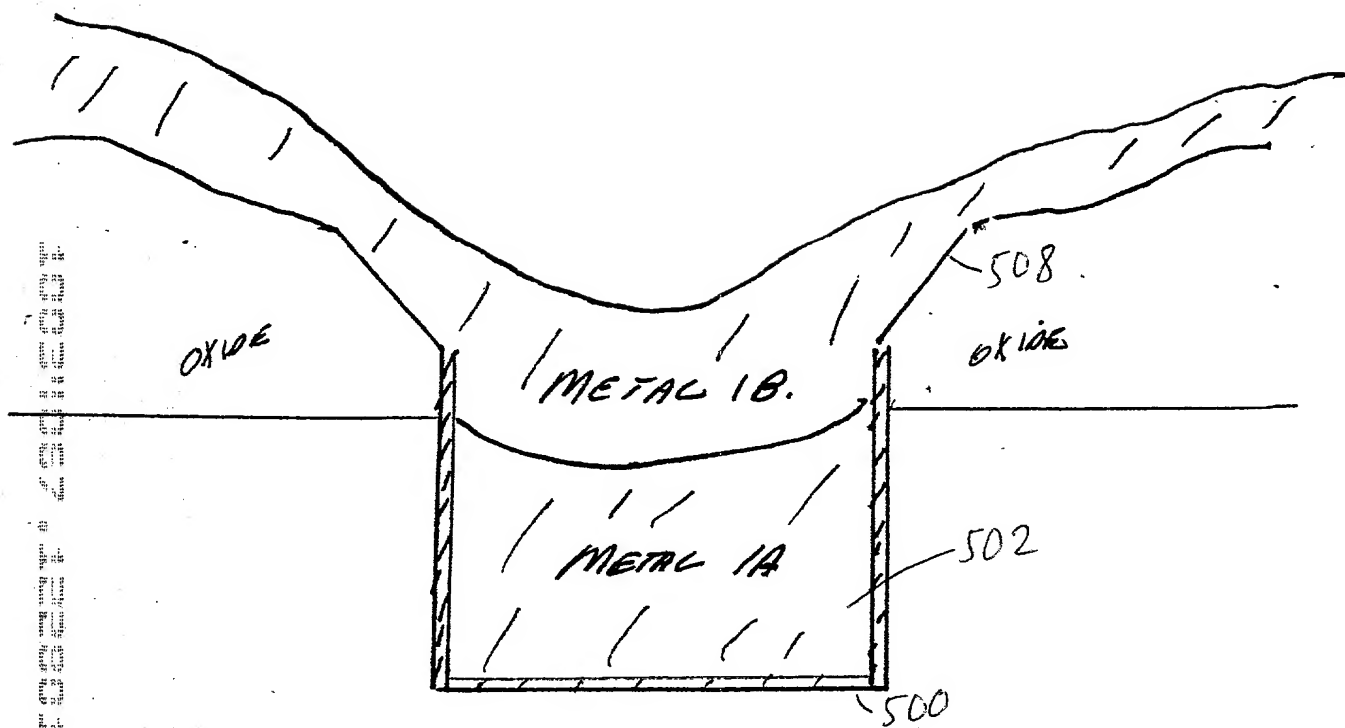
RESIST COATING - THICK IN THE  
SLOTS

Fig. 6



RESIST PLANNED ETCHED.  
 LEAVING RESIST IN FLOTS.  
 FIELD METAL ETCHED OFF.

Fig. 7



RESIST STRIPPED & SECOND  
METAL 1B SPUTTER DEPOSITED

Fig. 8

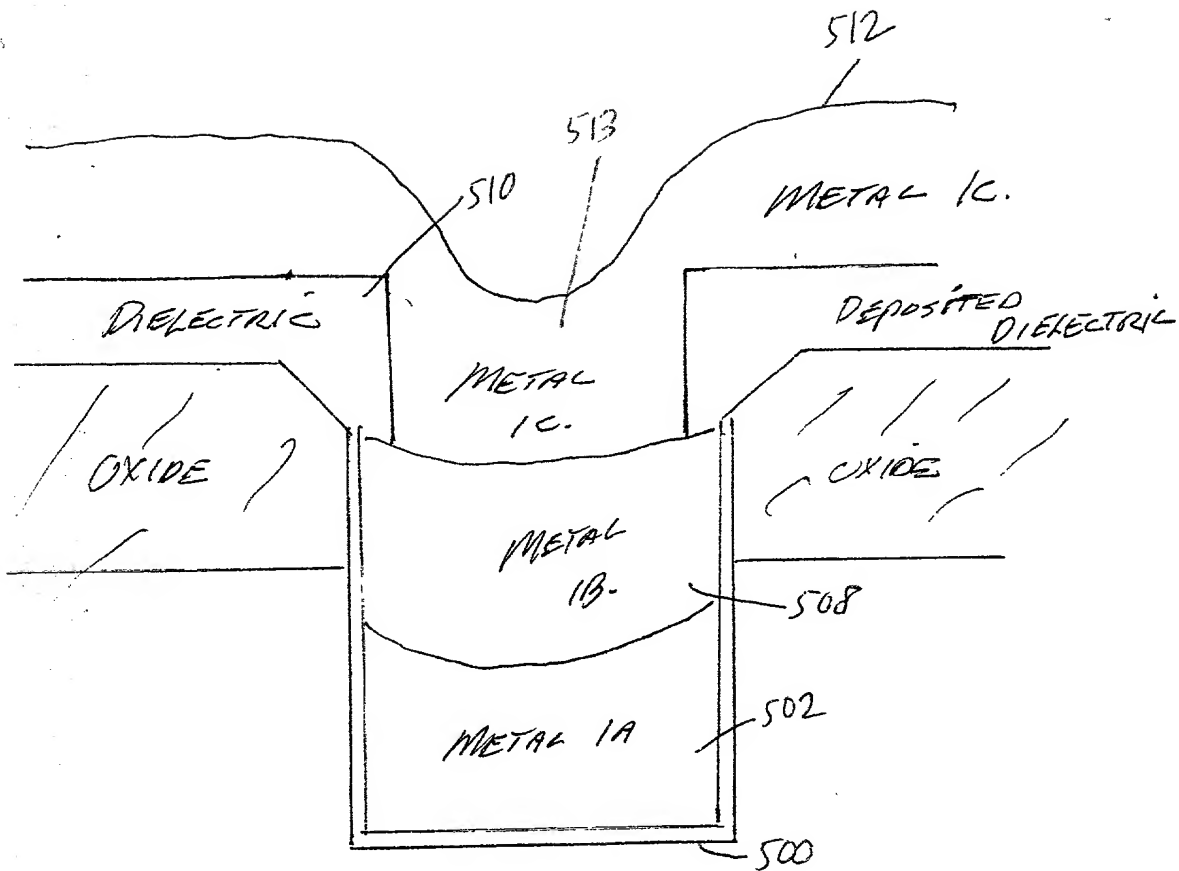


Fig. 9



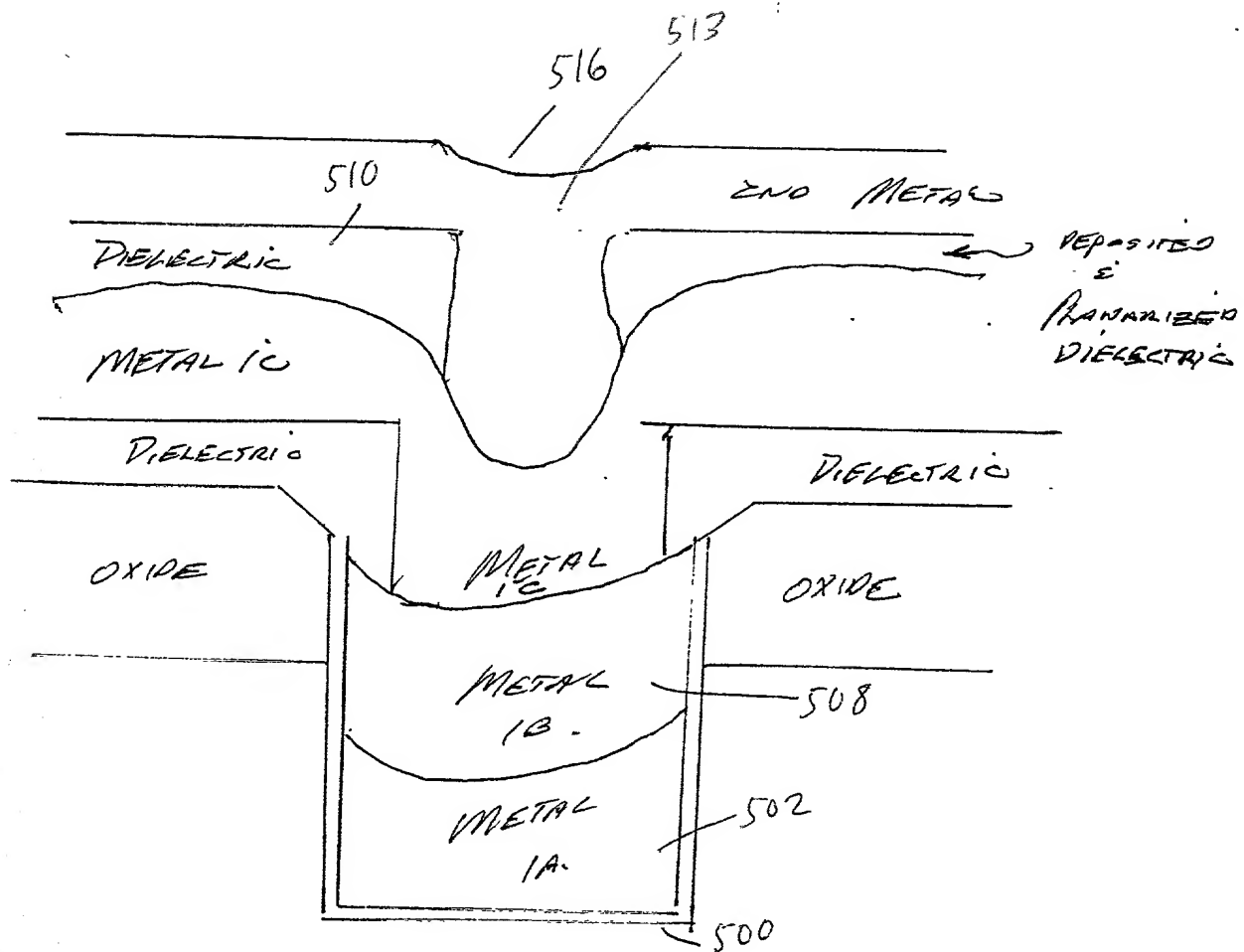
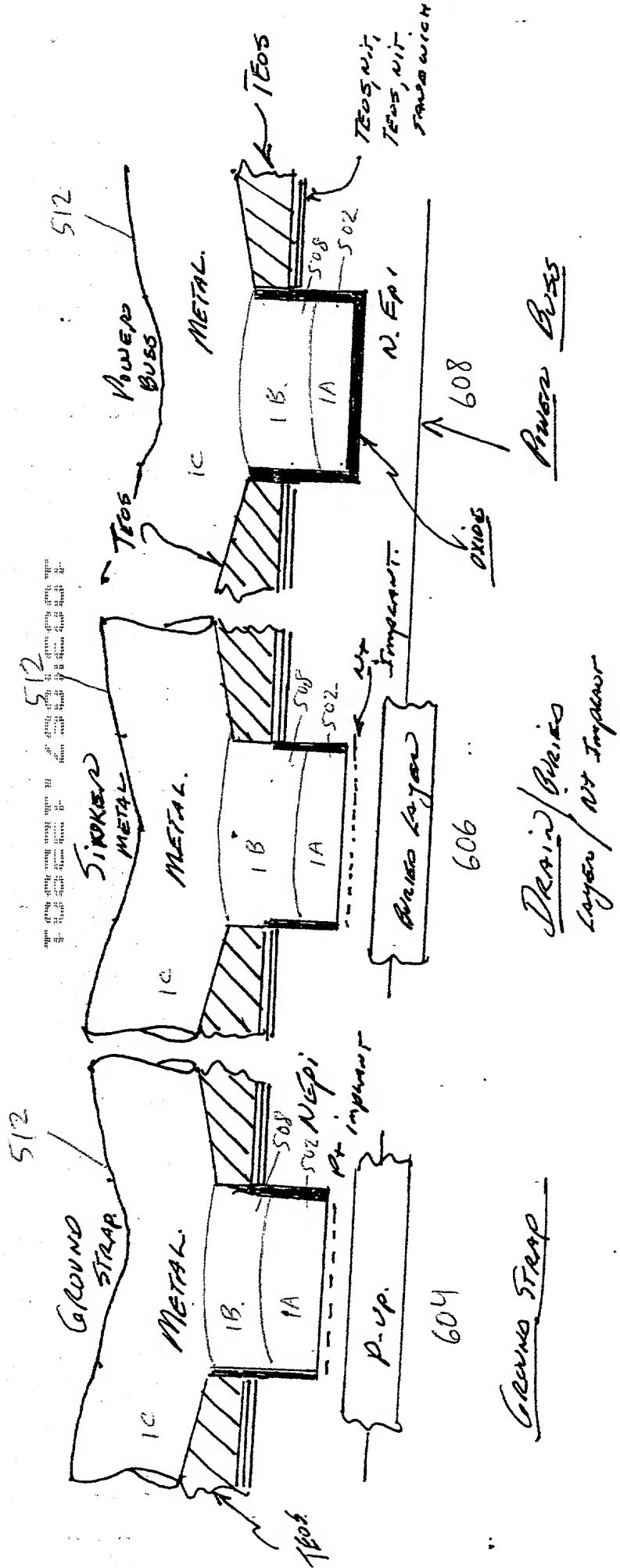


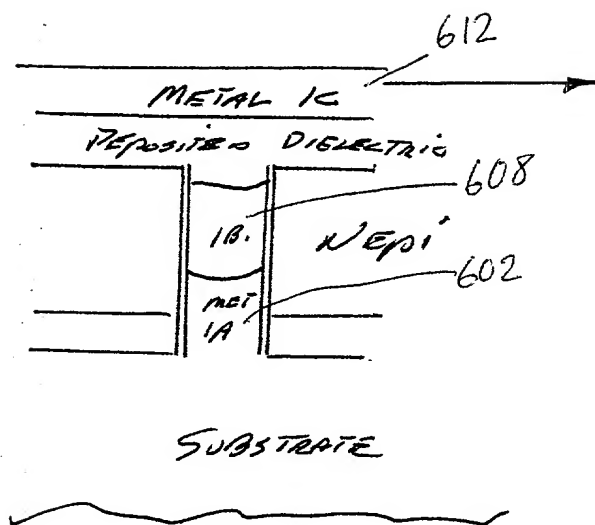
Fig. 10



GROUND STRAP / POWER BUSS / DRAIN METAL SINKERS

THIN OXIDE LAYER OF DIOSIDE  
 FOLLOWED BY 900Å TEOS - POLISH -  
 SLOTT MASK - METAL  
 METAL 1.5 - 2.0 um deposited

Fig. 11 Power Metal.



METAL 1C  
CONNECTS AN ISOLATED  
ISLAND TO ADJACENT  
ISOLATED EPI ISLANDS  
AND CROSSES OVER THE  
ISOLATION GROUND  
STRAP BY NOT OPENING  
A VIA IN THIS PORTION  
TO ALLOW 1C TO BE  
ISOLATED FROM GROUND.

Fig. 12